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501.39149X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: NAKAMURA et al.

Serial No.: 09/708,450

Filed: November 9, 2000

For: A SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE AND THE METHOD THEREOF

Group: 2811

Examiner: D. Owens

CONFIRMATION FILING OF APRIL 21 AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

April 29, 2003

Sir:

Applicants filed a responsive Amendment after Final Rejection and Petition for One Month Extension of Time on April 21, 2003. A copy of the U.S. post card showing the filing of this Amendment is attached. Additionally, hereto is a copy of the April 21 Amendment after Final Rejection and Petition for Extension of Time. These copies are merely being filed as confirmation copies of the previous filed documents. That is, these documents are identical to the previously filed documents. While these documents were timely filed on April 21, 2003, if any extension of time fee is necessary in order to enter these April 21 documents, then applicants petition for an extension of time under 37 C.F.R. §1.136. Please charge any fee in connection with an extension of time to account 01-2135 (referencing case no. 501.39149X00).

Respectfully submitted,

David C. Oren
Registration No. 38,694
ANTONELLI, TERRY, STOUT & KRAUS, LLP

DCO/pay

Patent Dkt. No. 501.39149X00 Attorney Initials GEM/DCO

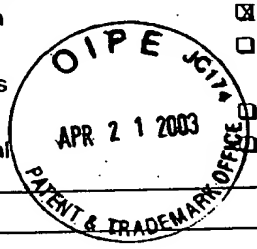
Application No. 09/708,450 Filing Date November 9, 2000

Applicant(s) NAKAMURA et al.

Papers Filed Herewith on April 21, 2003

Receipt is hereby acknowledged of the papers filed as indicated by the checked items in connection with the above-identified application:

- ☐ New Application Transmittal Form
  - ____ Pages of Specification (___ claims)
  - ____ Sheets of Drawings
- ☐ Declaration (___ pages)
- ☐ Fee Transmittal Form
- ☐ Claim for Priority
  - ☐ Priority Documents
- ☐ Assignment Papers
- ☐ Issue Fee Transmittal
- ☐ Other _____



- ☒ Credit Card Payment Form
  Fees $ 410.00
- ☒ Amendment
- ☐ Response to Office Action
- ☒ Petition for Extension of Time (2 mos.)
- ☐ Information Disclosure Statement
  - ☐ PTO-1449 ☐ Copies of References
- ☐ Revised Drawings (___ sheets)
- ☐ Notice of Appeal

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AMENDMENT AFTER FINAL REJECTION

BOX AF
Commissioner for Patents
Washington, D.C. 20231

April 21, 2003

Sir:

In response to the Office Action dated November 20, 2002, please amend the above-identified application as follows.

IN THE CLAIMS:

Please cancel claims 23 and 27 without prejudice or disclaimer.

Please amend claims 20-22, 24-26 and 28-34 as follows:

20. (Twice Amended) A method of producing a semiconductor integrated circuit device comprising the steps of:

(a) forming bit lines and a first layer wiring over MISFET on a main plane of a semiconductor substrate through a first inter-layer insulating film, forming a second inter-layer insulating film and an electrode-forming insulating film, and etching holes in said electrode-forming insulating film;